HIGH-PERFORMANCE CLOCK-POWERED LOGIC

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Cross-Reference to Related Applications

This application claims the benefit of the filing date of U.S. Provisional Application No. 60/144,520, entitled "High-Performance Clock-powered Logic," filed July 19, 1999, and U.S. Provisional Application No. 60/174,509 entitled "A Low-Power SRAM With Resonantly Powered Data, Address, Word and Bit Lines," filed January 5, 2000, the contents of both of which are incorporated herein by reference.

Background of Invention

Field of the Invention

This invention relates to digital systems and, more particularly, to digital systems that are driven by clock-powered logic, including adiabatic signals.

Description of Related Art

Digital systems include signal lines that carry digital signals, including data lines, address lines and control lines.

In many instances, these signal lines are much longer than the distances between the integrated circuitry components. Such long signal lines are commonly used to connect the various subsystems in an integrated circuit, as well as the pixels in an LCD display.

One of the primary problems with long signal lines is the substantial capacitance which they impose. As is well known, the presence of this substantial capacitance causes a corresponding substantial loss in energy while the signal lines are being driven between one logic state and another, such as commonly occurs during the serial delivery of digital data over the signal lines.

One attempt to minimize these energy losses is to use what has become known as a "clocked buffer." In a typical digital system, the digital signal powers one end of a signal line by controlling switches that switch the end of the signal line between the supply voltage (typically logic "1") and ground (typically logic "0"). With a clocked buffer, on the other hand, the digital signal is instead used to control the delivery of a clock signal into the input of the signal line.

If this clock signal rises and falls slowly, energy will be saved, particularly when energy stored in the capacitance of the signal lines is returned to a temporary storage device for re-use during the next clock cycle. The use of a slowly rising and falling signal to power a digital system has become known as adiabatic charging and discharging. Examples of such signals are described in U.S. Patents 5,559,478 and 5,473,526.

Unfortunately, the use of clocked buffers to power logic has, in the past, had some drawbacks.

First, the circuitry usually requires the voltage of the clock signal to exceed the supply voltage, i.e., for the clock signal to run "hot." This may stress certain digital devices by forcing them to run at voltage levels beyond the levels for which they were designed. The excessive voltages, moreover, tend to offset the energy savings realized from the clock-powered approach, since energy loss increases as the square of the voltage increase.

A second problem with existing clock-powered logic is that it often reduces the speed at which the logic circuitry can be clocked. Generally, the existing clock-powered logic systems require the logic circuitry to process the incoming digital signals and to generate an appropriate output signal within no more than one-half of the period of the clock signal and, in many cases, on even a faster basis. This increases the required speed of the logic circuitry or, in the alternative, reduces the maximum speed of the clock signal.

Solutions to the problems of excessive clock signal voltage and insufficient processing time, moreover, have usually worked against one another. One way to reduce the adverse consequences of "hot clocks" is to reduce the voltage of these clocks. Reducing clock signal voltage, however, usually reduces processing speed, thereby requiring clock signal speed to be even further reduced. Conversely, the speed at which the logic processes its signals can usually be increased by increasing the voltage of the

clock signal. Unfortunately, this increases concerns over device stress and energy dissipation.

In short, there continues to be a need in the art for clock-powered logic that maximizes the conservation of energy without stressing devices, nor slowing system performance.

Summary of Invention

One object of the invention is to obviate these as well as other problems in the prior art.

Another object of the invention is to reduce energy consumption in digital systems.

A still further object of the invention is to increase the speed at which digital systems can operate.

A still further object of the invention is to reduce stress on digital circuitry components.

A still further object of the invention is to provide more time for digital logic circuitry to process signals, without slowing clock signal speed.

A still further object of the invention is to reduce the voltage of clock-powered logic.

These, as well as still further features, objects and benefits of the invention, are achieved through the use of various circuitry components, configurations and processing methods.

In one embodiment of the invention, a signal level booster has an input configured to be in communication with a signal that is reflective of the input digital signal. The booster also has an output that is reflective of the input to the signal level booster, but of greater magnitude.

A first latch has an input in communication with the output of the signal level booster. It is configured to be toggled by the output of the signal level booster and by a first clock signal. The first latch also has an output.

Digital logic has an input in communication with a signal that is reflective of the output of the first latch. The digital logic also has an output.

A second latch has an input in communication with the output of the digital logic. It is configured to be toggled by the output of the digital logic and by the first clock signal. The second latch has an output configured to deliver the output digital signal.

In one embodiment, a jam latch functions as the signal level booster and as the first latch. The second latch may also include an n-latch.

In one embodiment, the input digital signal and the output digital signal are each a single signal. In another embodiment, they are a complementary pair of signals.

In a still further embodiment, a clocked buffer is configured to be powered by a second clock signal that is complementary to and substantially substantially non-overlapping with the first clock signal. The clocked buffer has an input configured to be in communication with the input digital signal. It also has an output in communication with the signal level booster.

Preferably, the second clock signal is an adiabatic signal. The adiabatic signal may include blips, a staircase signal or a ramp signal.

In a still further embodiment, a third latch is provided having an input in communication with the output of the first latch. The third latch is configured to be toggled by the output of the first latch and by the second clock signal. The third latch has an output in communication with the input to the digital logic. The third latch may include an n-latch.

The invention also includes methods of signal processing, including methods implemented by the circuitry discussed above.

The invention also includes other structures, methods, features and benefits, as will now become clear from a review of the following detailed description of the preferred embodiments and the attached drawings and claims.

Brief Description of Drawings

FIG. 1 is a block diagram of the architecture of a typical prior art clock-powered logic system.

FIG. 2 is a block diagram of the prior art energy recovery latch shown in FIG. 1.

FIG. 3. is a graph of the prior art complementary and substantially substantially non-overlapping clock signals generated by the clock driver shown in FIG. 1.

FIG. 4 is a typical prior art circuit for the prior art clocked buffer shown in FIG. 2.

FIG. 5 is a graph of two of the signals that are typically generated by the prior art circuit shown in FIG. 4.

FIG. 6 is a diagram of some of the typical prior art components relating to the prior art digital logic shown in FIG. 1.

FIGS. 7 (a) – (c) are graphs of other typical prior art adiabatic signals that may be used in the prior art clock-powered logic shown in FIG. 1.

FIG. 8 is a block diagram of one embodiment of the invention.

FIG. 9 is one embodiment of a circuit of the invention that is shown in FIG. 8.

FIG. 10 is a block diagram of another embodiment of the invention using complementary input signals, but only a single latch between the clocked buffer and the digital logic.

FIG. 11 is a circuit of one embodiment of the level booster and latch shown in FIG. 10.

FIG. 12 is a block diagram of another embodiment of the invention that does not use two latches between the clocked buffer and the digital logic, nor complementary digital input signals.

Detailed Description of Preferred Embodiments

FIG. 1 is a block diagram of the architecture of a typical prior art clock-powered logic system.

As shown in FIG. 1, the digital signal to be processed, D_{in} in this example, is delivered to an energy recovery latch **1**. The output of the energy recovery latch **1** is delivered to digital logic **3**.

Digital logic **3** represents the digital logic that processes the signal received from the energy recovery latch **1**, typically over a long signal line, such as signal line **4**.

The output of the digital logic **3** is delivered to a second energy recovery latch **5**. The output of the second energy recovery latch **5** is delivered to a second set of digital logic **7**. This architecture repeats until the digital signal, D_{in}, is processed by all of the needed digital logic, leading to the generation of the output digital signal, D_{out} in this example. The energy recovery latches, including latches **1** and **5**, operate under the control of a clock driver **9**.

FIG. 2 is a block diagram of the prior art energy recovery latch **1** shown in FIG. 1. As shown in FIG. 2, the prior art energy recovery latch **1** includes a latch **21** and a clocked buffer **23**. A capacitor **25** is included to illustrate the capacitance that the signal line **4** imposes.

FIG. 3 is a graph of the complementary and substantially substantially non-overlapping clock signals ϕ_A and ϕ_D generated by the prior art clock driver **9** shown in FIG. 1, the partial routing of which are shown in FIG. 2. The phrase "substantially substantially non-overlapping" is used to indicate that a small degree of overlap is permissible.

FIG. 4 is a typical prior art circuit of the prior art clocked buffer **23** shown in FIG. 2. As shown in FIG. 4, the latched data, illustrated in Fig. 4 as $\overline{D_{inL}}$, is delivered to an inverter **41** and then to an electronic switch **43**. V_{iso} represents a reference voltage which, as will soon be seen, is quite high.

In operation, D_{out} reflects the complementary clock signal phase ϕ_B when $\overline{D_{inL}}$ is low. This occurs through the operation of electronic switch **43**, as well as electronic switches **45** and **47**. In essence, the clock signal ϕ_B becomes buffered and metered by the data signal.

FIG. 5 is a graph of two of the signals that are typically generated by the prior art circuit shown in FIG. 4, namely D_{out} and D_{bn}. As seen in FIG. 5, D_{bn} must rise above the level of D_{out} during the cycle. Because D_{out} is typically at the supply level, this usually means that D_{bn} is above the supply level and, as a consequence, that ϕ_B must be above the supply level.

This excessive voltage in ϕ_B is known as a "hot clock" and, as explained above, is undesirable. It potentially places stress on the components in the system and increases energy dissipation. Even greater stress is placed on the devices connected to D_{bn}.

FIG. 6 is a diagram of some of the typical prior art components relating to the prior art digital logic shown in FIG. 1. Clocked buffer **61** is just one of many clocked buffers that are used in the system, such as the one illustrated in FIG. 2. Electronic switches **63** and **65** form a latch that is controlled by the output of the clocked buffer **61** and the clocked signal ϕ_A. The output of this latch is inverted by an inverter **67** and delivered to digital logic circuitry **69**. In order to preserve the state of the digital logic circuitry **69** after processing input data, the output of the digital logic circuitry **69** is

delivered to an electronic switch **71** and to an inverting buffer **73**. The output of the inverting buffer **73** is then again delivered to a clocked buffer **75** to generate D_{out}.

In order to ensure the proper functioning of the inverting buffer **73**, the input to the inverting buffer **73** must be at near-supply level during its logic "1" state. In turn, this requires the voltage of the clock signal ϕ_A to be above the supply level, just like with ϕ_B. This again raises concerns over circuitry stress and increases energy dissipation.

As explained above, another problem with the clock-powered logic in the prior art is that the digital logic circuitry must operate very quickly. More specifically, the digital logic **69** must operate fast enough to generate an output by the time its input signal is removed. In the typical prior art circuit, the input signal to the digital logic **69** begins on the rising edge of clock signal ϕ_B and ends on the falling edge of clock signal ϕ_B. In order to generate a stable output during this interim, the digital logic **69** must either be very fast or the clock signal ϕ_B must be very slow. Neither approach is desirable.

To maximize energy conservation, the clocks should rise and fall as slowly as possible. Signals with slow rising and falling edges have become known as adiabatic signals. Thus far, one form of slowly rising and falling edges has been shown in FIG. 3. Another form is a blip signal, as shown in FIG. 7(a). Another form is a staircase signal, as shown in FIG. 7(b). A still further form is a ramp signal, as shown in Fig. 7(c). A circuit for generating the blip signal shown in FIG. 7(a) is disclosed in U.S. Patent 5,559,478. A circuit for generating the staircase signal shown in FIG. 7(b) is shown in U.S. Patent 5,473,526. The content of both of these patents is incorporated herein by reference.

FIG. 8 is a block diagram of one embodiment of the invention. As will soon be seen, FIG. 8 represents clock-powered logic that utilizes a clock signal that is below the supply voltage, without sacrificing speed. Further, the system shown in FIG. 8 allows the clock signal speed to be faster, without increasing the speed of the logic.

As shown in FIG. 8, a digital signal, such as D_{in}, is used to control a clocked buffer **101** that operates under the control of a clock signal ϕ_B. The clocked buffer **101** is the same as the clocked buffers shown in the prior art, except that it produces a clocked signal of lower voltage and does not require a "hot clock."

A level booster **103** receives the clocked signal from the clocked buffer **101** and boosts its level. The output of the level booster **103** is delivered to a latch **105** that

operates under the control of the clock signal ϕ_A. The output of the latch **105** is delivered to a second latch **107** that operates under the control of the clock signal ϕ_B. The output of the latch **107** is delivered to digital logic **109**. Digital logic **109** is any form of digital logic, including data processing circuitry, memory, control circuitry, and addressing circuitry.

The output of the digital logic **109** is delivered to a third latch **111** that operates under the control of the clock signal ϕ_A. The output of the latch **111** represents the final processed digital signal D_{out}.

The data signals, D_{in} and D_{out}, are merely representative of the types of digital signals that the invention can process. The invention is equally useful in connection with all other types of digital signals, such as digital signals representing addresses or control.

The clock signals ϕ_A and ϕ_B are preferably the same type of complementary and substantially non-overlapping clock signals that were discussed above in connection with the prior art, namely the trapezoid signals shown in FIG. 3, or the blips, staircase or ramp signals shown in FIG. 7. Other adiabatic wave shapes can also be used. Indeed, the invention is also applicable to fast-rising, non-adiabatic signals, although it is anticipated that there would be less energy recovery with such signals. Even overlapping clock signals could be used, although the circuitry would have to be different.

Although having illustrated only one segment of digital logic, digital logic **109**, the clock-powered logic shown in FIG. 8 is often repeated, much like the architecture that is shown in FIG. 1. FIG. 8 is intended to merely illustrate the overall topology of a section of the typical clock-powered logic system that incorporates the invention.

FIG. 9 is a circuit of one embodiment of the invention shown in FIG. 8.

The clocked buffer **101** can be the same circuit as was discussed above in connection with the clocked buffer of the prior art, such as the circuitry shown in FIG. 4. As will soon be seen, however, the invention does not require a "hot clock." Thus, the magnitude of the voltage of ϕ_B (as well as ϕ_A, as will be seen later) can be below the supply voltage. This is accomplished with an appropriate reduction in V_{iso} (see FIG. 4), as should be readily apparent to the skilled artisan.

A capacitor **121** reflects the capacitance that is exhibited by the signal line **120** over which the clocked signal from the clocked buffer **101** is delivered. The signal line

120 is usually long with respect to the distances between the circuitry components in the digital logic **109**; however, this is not a requirement of the invention.

The level booster **103** and the latch **105** in FIG. 8 are implemented in FIG. 9 by a single jam latch **123**. As should be obvious to those skilled in the art, the jam latch **123** is set by a rising edge from the clocked buffer **101** and reset by a rising edge from the clock signal ϕ_A. As is known, a jam latch is an example of a device that converts a pulse to a level and also boosts the level of the signal. Other devices that perform one or more of these functions could also be used, albeit with varying results.

The output of the jam latch **123** is then delivered to an n-latch **125** that implements the latch **107** shown in FIG. 8. The n-latch is set by a rising edge from the output of the jam latch **123** and reset by a rising edge from the clock signal ϕ_B. As is known, an n-latch is an example of a device that can be clocked by a small-swing signal. Other devices that perform this function could be used instead.

The output of the n-latch **125** is then delivered to the digital logic **109**, which is the same as the digital logic **109** shown in FIG. 8. The output of the digital logic **109** is then delivered to a second n-latch **127** that preserves the output of the digital logic **109** under the control of the clock signal ϕ_A. The output of the n-latch **127** is then delivered as the output data, D_{out}.

The advantages of this configuration over the prior art configuration shown in FIG. 1 should now be apparent. First, the level boosting function of the jam latch **123** allows the system to function with a low clock signal voltage. Second, the use of two latches, the jam latch **123** and the n-latch **125**, prolongs the period during which the clocked data signal is delivered to the digital logic **109** for almost a complete clock signal cycle, thereby giving the digital logic **109** far more time to develop the necessary output before the input signal is removed. Further, all of these functions are also achieved with a clock signal voltage that is below the supply voltage.

FIG. 10 is a block diagram of another embodiment of the invention using complementary input signals, but only a single latch between the clocked buffer and the digital logic. As shown in FIG. 10, a complementary clocked buffer **141** receives complementary data signals and, under the control of clock signal ϕ_B, delivers complementary clocked buffer outputs to a complementary level booster **143**. In turn, the output of the complementary level booster **143** is delivered to a complementary latch

145. The output of the complementary latch **145** is delivered to complementary digital logic **147**. The output of the complementary digital logic **147** is delivered to a complementary latch **149**. The output of the complementary latch is a complementary set of D_{out}. The complementary latch **149** is operated under the control of clock signal ϕ_A.

The use of these complementary signals enables the embodiment of FIG. 10 to essentially achieve all of the advantages and benefits of the embodiment of FIG. 8, without the second latch **107** that is shown in FIG. 8. Unlike the embodiment in FIG. 8, the first latch **145** in FIG. 10 is reset by the complementary clocked and boosted signal, as opposed to being reset by ϕ_A, as is the first latch **105** in FIG. 8.

FIG. 11 is a circuit of one embodiment of the level booster **143** and the latch **145** that is shown in FIG. 10. As can be seen in FIG. 11, the complementary output of the clocked buffer **141** is used to control a jam latch **151** that is included as a component. Because the jam latch **151** is no longer reset by the clock signal ϕ_A, as it was in FIG. 9, the output of the latch intrinsically remains high throughout the clock signal period, thus giving the digital logic **147** more time for processing, without the addition of a second latch, such as the latch **107** shown in FIG. 8.

FIG. 12 is a block diagram of a still further embodiment of the invention that does not use two latches between the clocked buffer and the digital logic, nor complementary data signals. This configuration is essentially the same as the one shown in FIG. 8, except that the second latch **107** is missing. With this configuration, the digital logic **109** is not given more time to process the input signal than it was given in the prior art circuit shown in FIG. 1. On the other hand, the system of FIG. 12 still eliminates the need for "hot clocks."

The embodiments of the invention that thus-far been described are for illustration purposes only. The invention is not limited to these embodiments. Rather, the invention encompasses a broad variety of other embodiments and signal processing approaches and is limited solely by the claims that now follow.

CLAIMS

1. A digital system for receiving an input digital signal and for generating an output digital signal that is related to the input digital signal comprising:

a) a signal level booster having an input configured to be in communication with a signal that is reflective of the input digital signal and an output that is reflective of the input to said signal level booster, but of greater magnitude;

b) a first latch having an input in communication with the output of said signal level booster, configured to be toggled by the output of said signal level booster and by a first clock signal, and having an output;

c) digital logic having an input in communication with a signal that is reflective of the output of said first latch and having an output; and

d) a second latch having an input in communication with the output of said digital logic, configured to be toggled by the output of said digital logic and by the first clock signal, and having an output configured to deliver the output digital signal.

2. The digital system of claim 1 in which a jam latch functions as said signal level booster and said first latch.

3. The digital system of claim 2 in which said second latch includes an n-latch.

4. The digital system of claim 1 in which said second latch includes an n-latch.

5. The digital system of claim 1 in which the input digital signal and the output digital signal are each a single signal.

6. The digital system of claim 1 in which the input digital signal and the output digital signal are each a complementary pair of signals.

7. The digital system of claim 1 further including a clocked buffer configured to be powered by a second clock signal that is complementary to and substantially non-overlapping with the first clock signal and having an input configured to be in communication with the input digital signal and having an output in communication with said signal level booster.

8. The digital system of claim 7 in which the second clock signal is an adiabatic signal.

9. The digital system of claim 8 in which the adiabatic signal includes blips.

10. The digital system of claim 8 in which the adiabatic signal includes a staircase signal.

11. The digital system of claim 8 in which the adiabatic signal includes a ramp signal.

12. The digital system of claim 8 in which the input digital signal is a complementary pair of signals and in which the input to said clocked buffer is configured to be in communication with the complementary pair of signals.

13. The digital system of claim 8 further including a third latch having an input in communication with the output of said first latch, configured to be toggled by the output of said first latch and by the second clock signal, and having an output in communication with the input to said digital logic.

14. The digital system of claim 13 in which said third latch includes an n-latch.

15. The digital system of claim 14 in which said jam latch functions as said signal level booster and said first latch.

16. The digital system of claim 15 in which said second latch includes an n-latch.

17. A method for generating an output digital signal that is related to an input digital signal comprising:

a) boosting an incoming signal that is reflective of the input digital signal;

b) latching the boosted signal under the control of a first clock signal;

c) processing a pre-processed signal that is reflective of the latched signal with digital logic;

d) latching the processed signal under the control of the first clock; and

e) delivering the latched processed signal as the output digital signal.

18. The method of claim 17 in which the input digital signal and the output digital signal are each a single signal.

19. The method of claim 17 in which the input digital signal and the output digital signal are each a complementary pair of signals.

20. The method of claim 17 further including clocking the input digital signal under the power of a second clock signal that is complementary to and substantially non-overlapping with the first clock signal and delivering this clocked signal as the incoming signal.

21. The method of claim 20 in which the second clock signal is an adiabatic signal.

22. The method of claim 21 in which the adiabatic signal includes blips.

23. The method of claim 21 in which the adiabatic signal includes a staircase signal.

24. The method of claim 21 in which the adiabatic signal includes a ramp signal.

25. The method of claim 21 in which the input digital signal is a complementary pair of signals and in which the clocked signal is based on the complementary pair of signals.

26. The method of claim 21 further including latching the latched signal under the control of the second clock signal and delivering that twice latched signal as the pre-processed signal.

27. A digital system comprising:

a) a clocked buffer;

b) a signal line having two ends, one end of which is in communication with said clocked buffer;

c) a jam latch in communication with the other end of said signal line;

d) digital logic in communication with said jam latch; and

e) a first n-latch in communication with said digital logic.

28. The digital system of claim 27 further including a second n-latch in communication with said jam latch and said digital logic.

29. The digital system of claim 28 wherein:

a) said jam latch and said first n-latch are controlled by a first clock signal; and

b) said clocked buffer and said second n-latch are controlled by a second clock signal that is complementary to and substantially non-overlapping with the first clock signal.

30. A clock-powered logic system containing logic configured to be connected to a supply voltage and configured to be powered by at least one clock having a voltage of a magnitude that does not exceed the magnitude of the supply voltage.

31. The clock-powered logic system of claim 30 in which said logic is configured to be powered by at least one clock having a voltage of a magnitude that is less than the magnitude of the supply voltage.

32. The clock-powered logic system of claim 30 in which said system includes a jam latch.

33. The clock-powered logic system of claim 30 in which said system includes a level booster circuit.

34. The clock-powered logic system of claim 30 in which said system includes a pulse-to- level converter.

35. The clock-powered logic system of claim 30 in which said system includes an n-latch.

36. The clock-powered logic system of claim 30 in which said system includes a device that can be clocked by a signal of smaller magnitude than the supply voltage.

37. The clock-powered logic system of claim 30 in which said system includes a clocked buffer.

38. The clock-powered logic system of claim 30 in which said system is configured to utilize an adiabatic signal.

39. The clock-powered logic system of claim 38 in which the adiabatic signal includes blips.

40. The clock-powered logic system of claim 38 in which the adiabatic signal includes a staircase signal.

41. The clock-powered logic system of claim 38 in which the adiabatic signal includes a ramp signal.

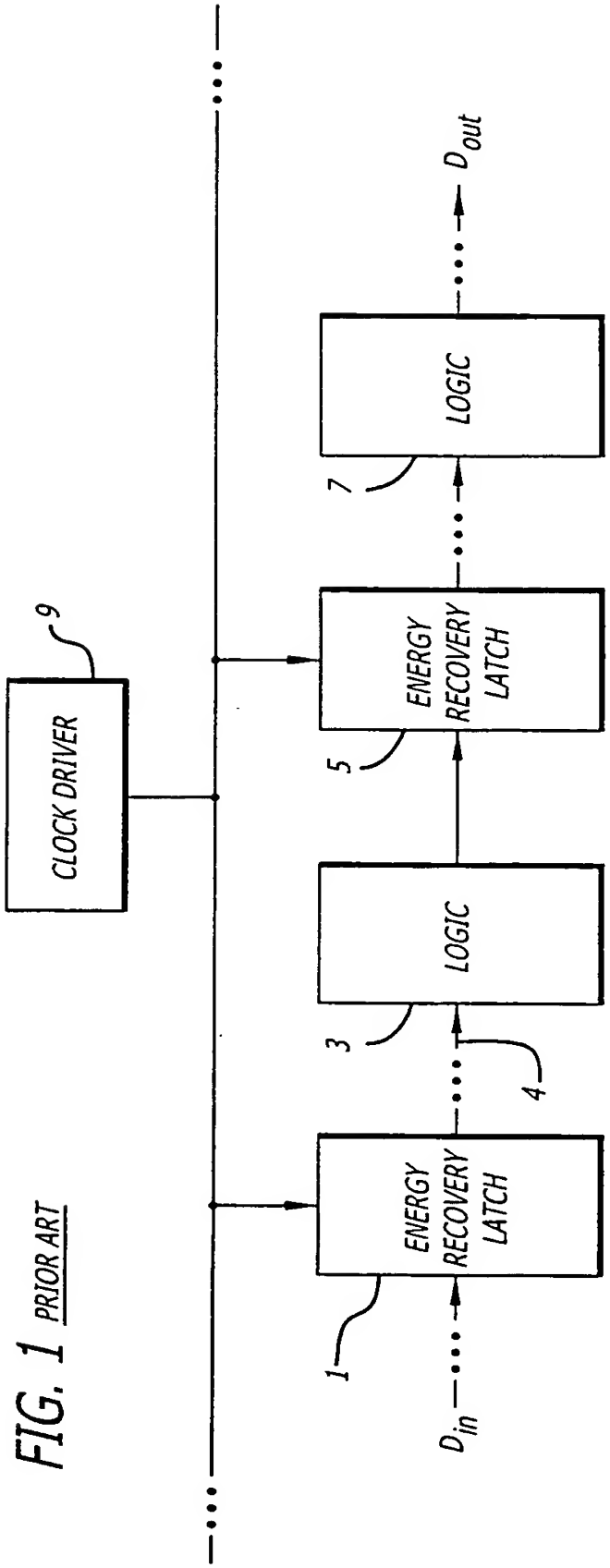


FIG. 1 PRIOR ART

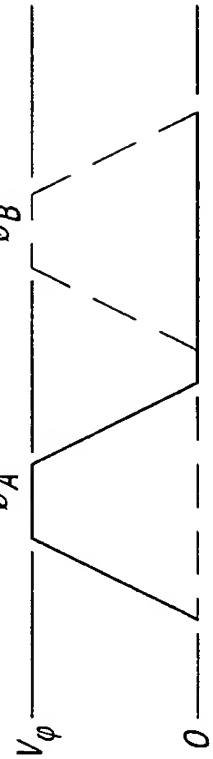


FIG. 3 PRIOR ART

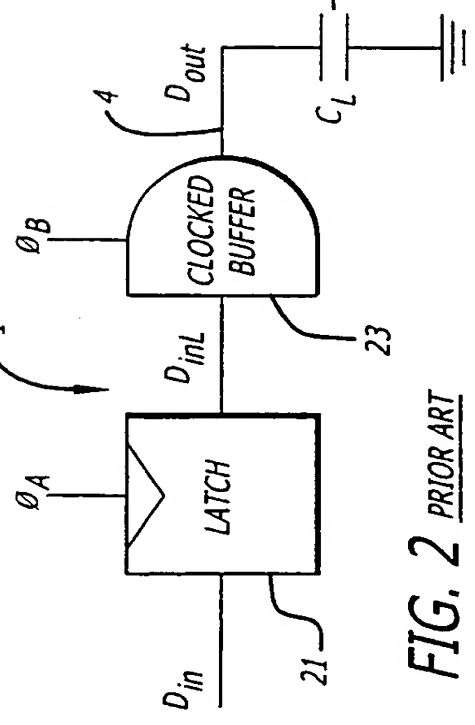


FIG. 2 PRIOR ART

FIG. 4 PRIOR ART

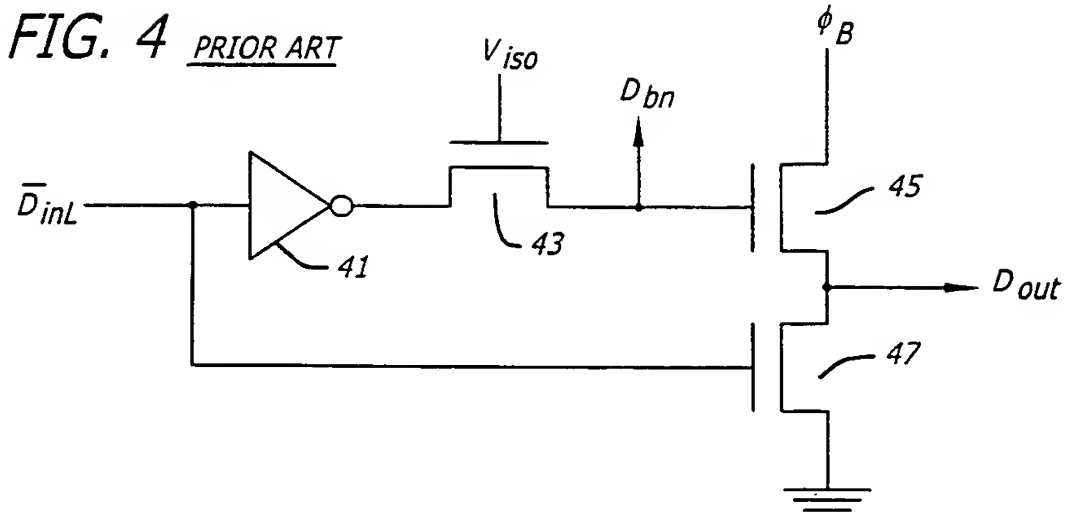
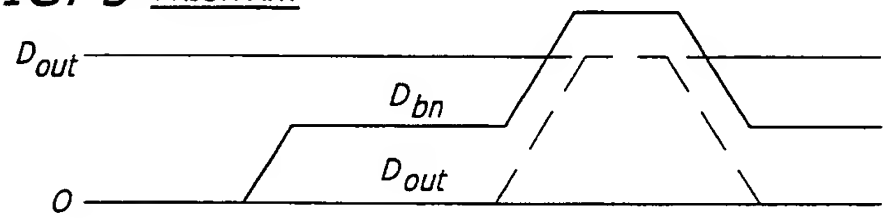


FIG. 5 PRIOR ART



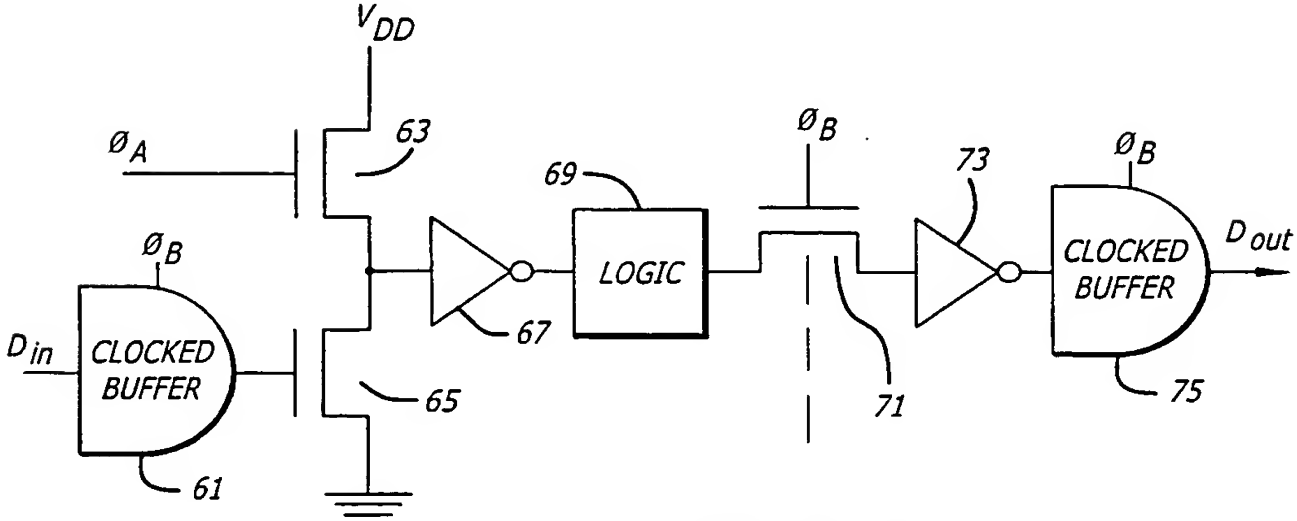


FIG. 6 PRIOR ART

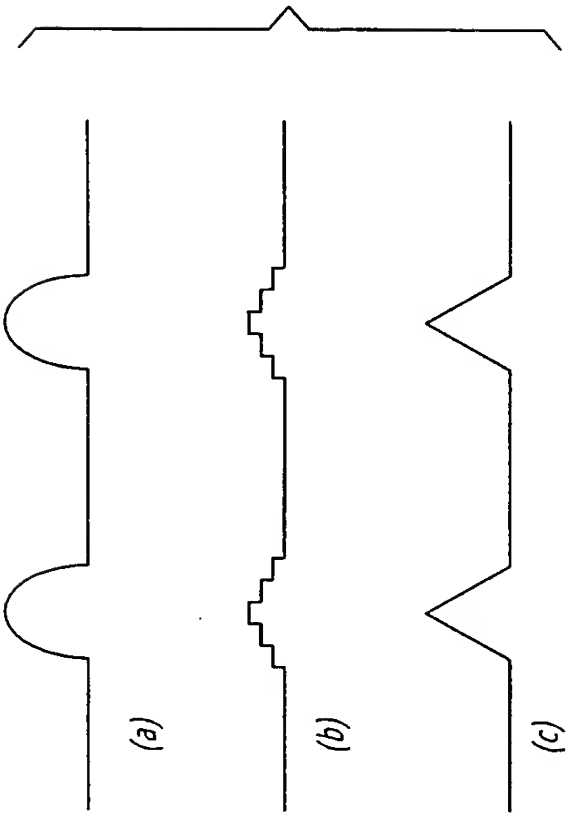


FIG. 7
PRIOR ART

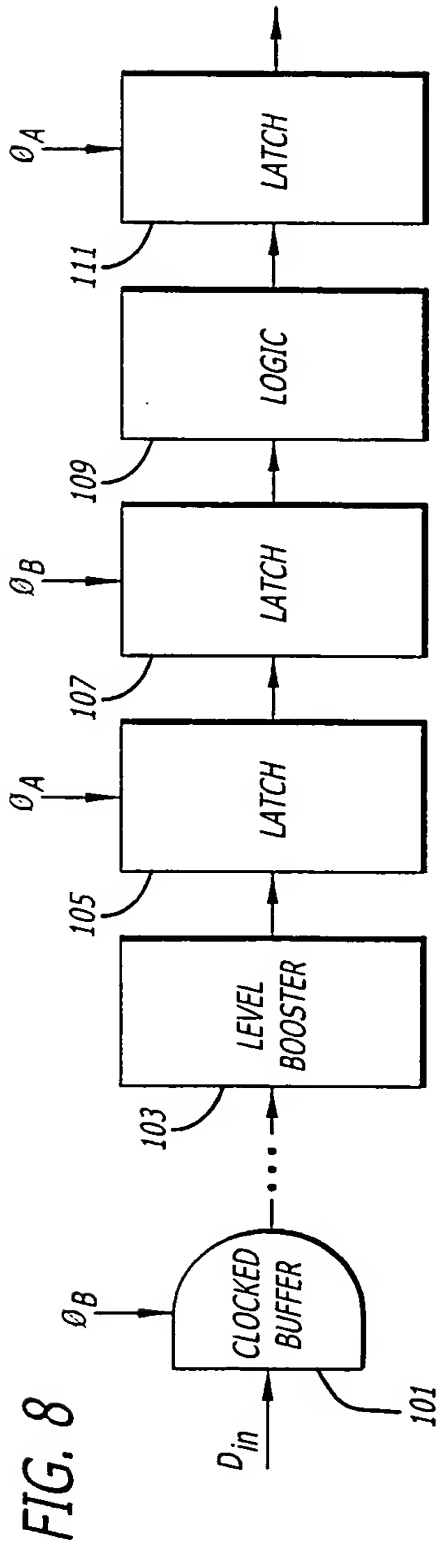


FIG. 8

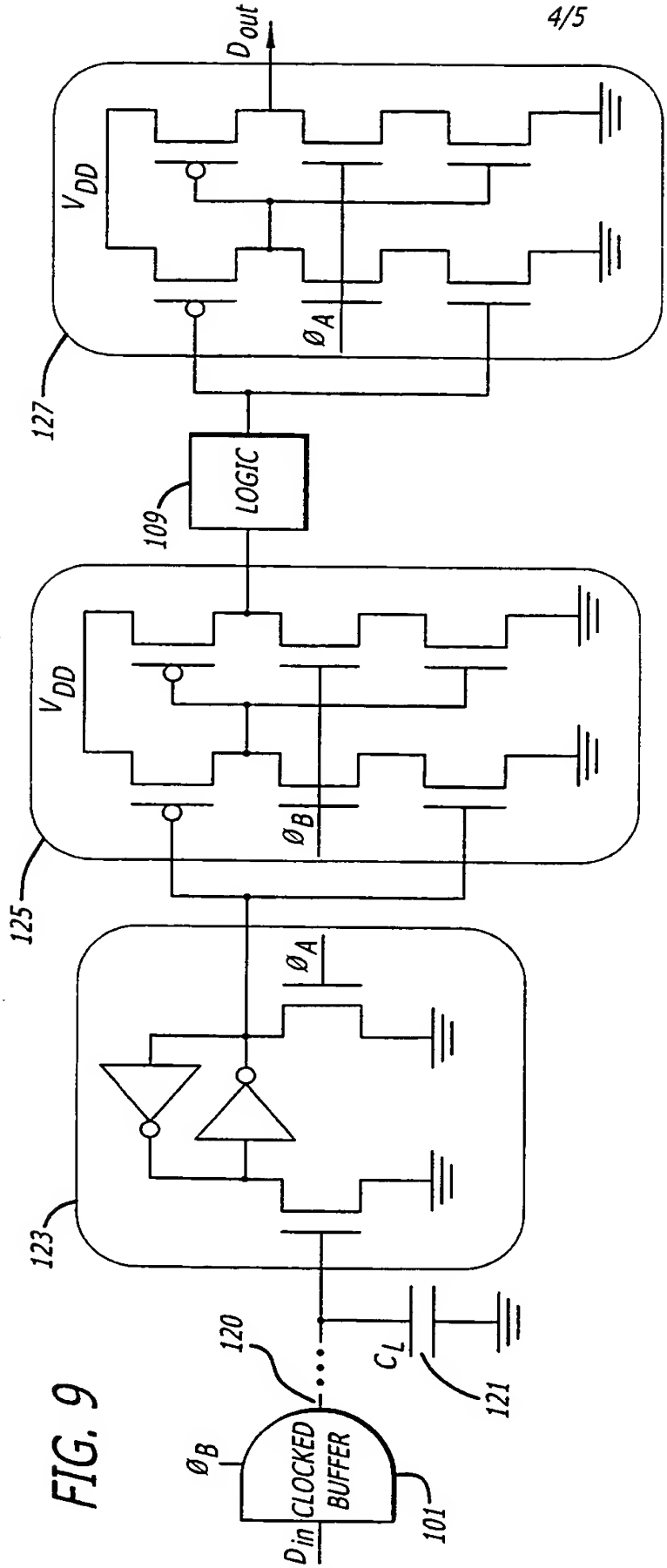

D_{out}
V_{DD}
ϕ_A
127
LOGIC
109
V_{DD}
ϕ_B
125
ϕ_A
123
120
C_L
121
ϕ_B
CLOCKED BUFFER
D_{in}
101

FIG. 9

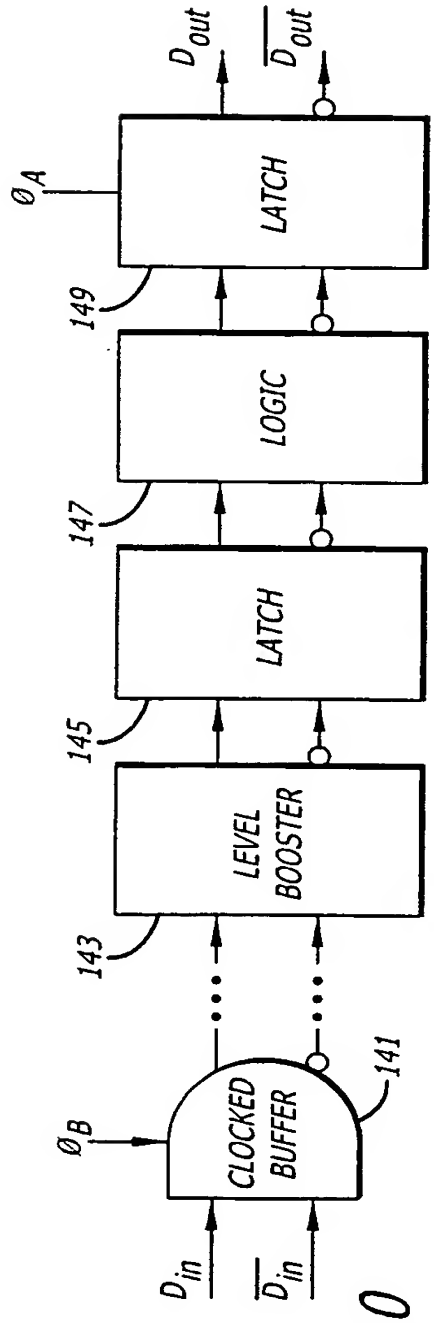

D_{out}
$\overline{D_{out}}$
ϕ_A
LATCH
149
LOGIC
147
LATCH
145
LEVEL BOOSTER
143
ϕ_B
CLOCKED BUFFER
141
D_{in}
$\overline{D_{in}}$

FIG. 10

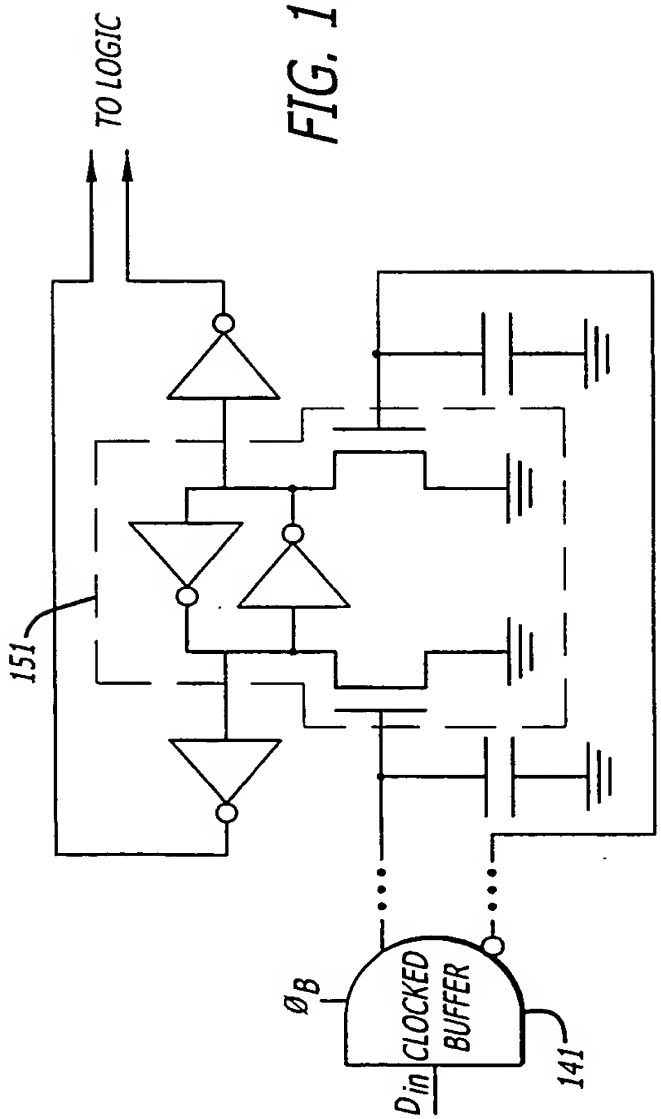

TO LOGIC
151
$\emptyset_B$
CLOCKED BUFFER
D_{in}
141

FIG. 11

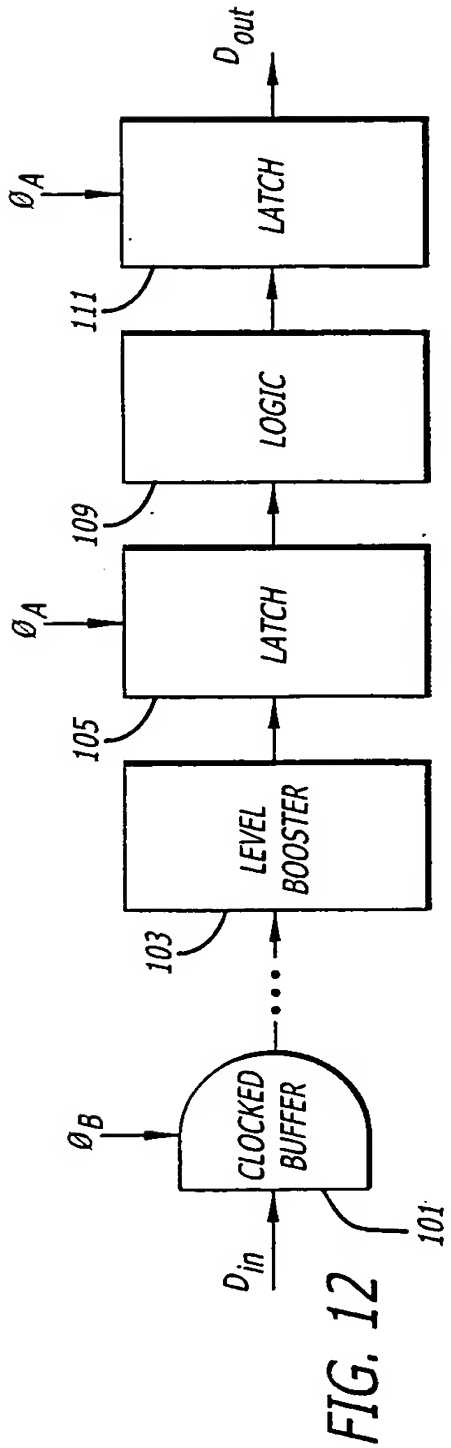

D_{out}
$\emptyset_A$
LATCH
111
LOGIC
109
$\emptyset_A$
LATCH
105
LEVEL BOOSTER
103
$\emptyset_B$
CLOCKED BUFFER
D_{in}
101

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/19608

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H03K 19/096
US CL :326/93, 98, 68; 327/225

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/93, 95, 96, 97, 98, 63, 68, 80, 81; 327/199, 211, 212, 215, 225

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST (USPAT, EPO, JPO)
search terms: flip-flop or latch, level shifter or booster, clock, clock powered logic.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	UK GB 2,248,988 A (SAMSUNG ELECTRONICS CO. LTD.), 22 April 1992, (22/04/92) all	1-41
X	US 5,504,441 A (SIGAL) 02 April 1996, (02/04/96) figure 3A.	30-31, 36
---		---
Y		1-5, 17-18, 27-28, 32-33, 35-37
A	US 5,646,555 A (MORINAKA) 08 July 1997, (08/07/97) figure 1.	1-41

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
14 SEPTEMBER 2000	10 OCT 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JON SANTAMAURO Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet) (July 1998)★

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 18036-24	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US00/19608	International filing date *(day/month/year)* 18 JULY 2000	Priority date *(day/month/year)* 19 JULY 1999
International Patent Classification (IPC) or national classification and IPC IPC(7): H05K 19/096 and US Cl.: 326/93, 98, 68; 327/225		
Applicant UNIVERSITY OF SOUTHERN CALIFORNIA ET AL.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 8 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand 12 FEBRUARY 2001	Date of completion of this report 31 DECEMBER 2001
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JAMES H. CHO Telephone No. (703) 308-0956

Form PCT/IPEA/409 (cover sheet) (July 1998)*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US00/19608

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-10, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of ____

[X] the claims:
pages 11-15, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of ____

[X] the drawings:
pages 1-5, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of ____

[X] the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of ____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language ____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages NONE

[X] the claims, Nos. NONE

[X] the drawings, sheets~~/fig~~ NONE

5. [ ] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US00/19608

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-29,32-34	YES
	Claims	30-31,35-41	NO
Inventive Step (IS)	Claims	2-3,7-16,20-29	YES
	Claims	1,4-6,17-19,30-41	NO
Industrial Applicability (IA)	Claims	1-41	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 30-31, 35-41 lack novelty under PCT Article 33(2) as being anticipated by Sigal (US PAT. 5,504,441).

Regarding claim 30, Sigal teaches a clock-powered logic system (see Fig. 12A) containing logic (see 121-125 in Fig. 12A) configured to be connected to a supply voltage (see Figs. 8 and 9) and configured to be powered by at least one clock (see CLOCK1 in Figs. 8, 9, and 12A) having a voltage of a magnitude that does not exceed the magnitude of the supply voltage (see col. 3, line 65+).

Regarding claim 31, Sigal teaches the clock-powered logic system of claim 30 where the logic is configured to be powered by at least one clock having a voltage of a magnitude that is less than the magnitude of the supply voltage (see col. 3, line 42+).

Regarding claim 35, Sigal teaches the clock-powered logic system of claim 30 where the system includes an n-latch (see Fig. 9).

Regarding claim 36, Sigal teaches the clock-powered logic system of claim 30 where the system includes a device (see Fig. 8) that can be clocked by a signal of smaller magnitude than the supply voltage (see col. 3, line 42+).

Regarding claim 37, Sigal teaches the clock-powered logic system of claim 30 where the system includes a clocked buffer (see the dynamic logic gate comprising P80, N80 and NMOSs in Fig. 8).

Regarding claim 38-41, Sigal teaches the clock-powered logic system of claim 30,but does not teach operating with an adiabatic signal or an adiabatic signal with blips or a staircase signal or a ramp signal as claimed. However, this limitation appears to be merely a statement of intended use of a logic circuit. It has been held that a recitation directed to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus

(Continued on Supplemental Sheet.)

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):
satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Claims 1, 4-6, 17-19 and 32-34 lack an inventive step under PCT Article 33(3) as being obvious over Sigal in view of Han (UK GB 2,248,988A).

Regarding claims 1 and 32-34, Sigal teaches a digital system of receiving an input digital signal and for generating an output digital signal that is related to the input digital signal comprising a first latch (see 120 in Fig. 12A) having an input from a circuit, configured to be toggled by the output of the circuit and by a first clock signal (see CLOCK1 in Fig. 21A) and having an output, and digital logic (see 121-125 in Fig. 12A) having an input in communication with a signal that is ref lective of the output of the first latch and having an output, and a second latch (see 126 in Fig. 12A) having an input in communication with the output of the digital logic and by the first clock signal and having an output configured to deliver the output digital signal, but does not teach a signal level booster having an input configured to be in communication with a signal that is reflective of the input digital signal and an output that is reflective of the input to the signal level booster but of greater magnitude.

However, Han teaches a signal level booster, a jam latch, or a pulse-to-level converter (see Fig. 3) having an input and an output having greater magnitude for the purpose of providing double voltage source interface circuit with reduced power consumption.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a signal level booster because it would provide an interface circuit with a reduced power consumption.

Regarding claim 4, Sigal teaches the digital system of claim 1 as discussed above and where the second latch includes an n-latch (see latch comprising N92, 94-97, NAND91 and 98, and P92-93 in Fig. 9)

Regarding claim 5, Sigal teaches the digital system of claim 1 as discussed above and the input digital signal and the output digital signal are each a single signal (see FROM LOG 2 and TO LOG 1 in Fig. 12A).

Regarding claim 6, Sigal teaches the digital system of claim 1 as discussed above and the input digital signal and the output digital signal are each a complimentary pair of signal (see Fig. 9).

The method claims 17-19 are essentially the same in scope as apparatus claims 1 and 4-6 and similarly lack an inventive step.

---------- NEW CITATIONS ----------